

## 1A Low Dropout Fast Response Positive Adjustable Regulator and Fixed 1.8V, 2.5V, 2.85V and 3.3V

### Features

- Guaranteed Output Voltage Accuracy within 2%
- Fast Transient Response
- Guaranteed Dropout Voltage at Multiple Currents
- Load Regulation : 0.1% Typ.
- Line Regulation : 0.03% Typ.
- Low Dropout Voltage : 1.1V Typ. at  $I_{OUT} = 1A$
- Current Limit : 1A Typ. at  $T_J = 25^\circ C$
- On-Chip Thermal Limiting :  $150^\circ C$  Typ.
- Adjustable Output : 1.25~10.7V
- Standard 3-pin TO-220, TO-252, TO-263 and SOT-223 Power Packages
- Lead Free Available (RoHS Compliant)

### Applications

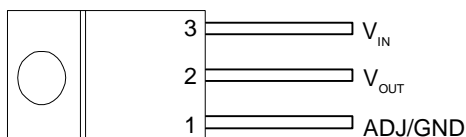
- Active SCSI Terminators
- Low Voltage Logic Supplies
- Post Regulator for Switching Power Supply

### General Description

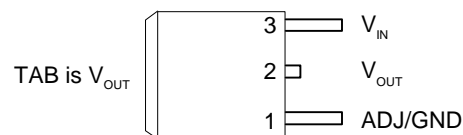
The APL1117 is a low dropout three-terminal adjustable regulators with 1A output current capability. In order to obtain lower dropout voltage and faster transient response, which is critical for low voltage applications, the APL1117 has been optimized. The device is available in an adjustable version and fixed output voltages of 1.8V, 2.5V, 2.85V and 3.3V. The output available voltage range of an adjustable version is from 1.25~10.7V with an input supply below 12V. Dropout voltage is guaranteed at a maximum of 1.3V at 1A. Current limit is trimmed to ensure specified output current and controlled short-circuit current. On-chip thermal limiting provides protection against any combination of overload that would create excessive junction temperatures. The APL1117 is available in the industry standard 3-pin TO-220, TO-252, TO-263, and the low profile surface mount SOT-223 power packages which can be used in applications where space is limited.

### Pin Description

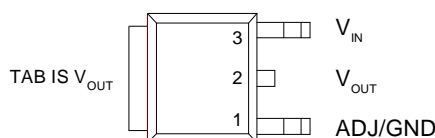
Front View for TO-220



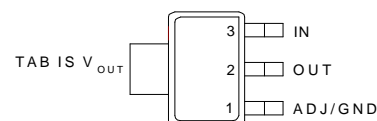
Front View for TO-263



Front View for TO-252

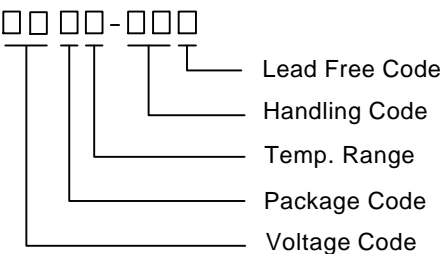

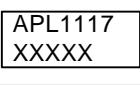

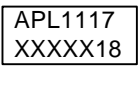

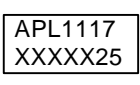
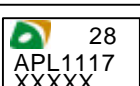
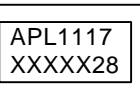
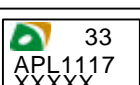
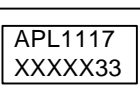


Front View for SOT-223



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

## Ordering and Marking Information

<p>APL1117- □□□□-□□□□</p>  <p>Lead Free Code Handling Code Temp. Range Package Code Voltage Code</p>	<p>Package Code F : TO-220 G : TO-263 U : TO-252 V : SOT-223 Temp. Range C : 0 to 70°C Handling Code TU : Tube TR : Tape &amp; Reel Voltage Code 18 : 1.8V      25 : 2.5V      28 : 2.85V 33 : 3.3V      Blank : Adjustable Version Lead Free Code L : Lead Free Device      Blank : Original Device</p>
<p>APL1117 F/G/U :  XXXXX - Date Code</p>	<p>APL1117 V :  XXXXX - Date Code</p>
<p>APL1117-18F/G/U :  XXXXX - Date Code</p>	<p>APL1117-18V :  XXXXX - Date Code</p>
<p>APL1117-25F/G/U :  XXXXX - Date Code</p>	<p>APL1117-25V :  XXXXX - Date Code</p>
<p>APL1117-28F/G/U :  XXXXX - Date Code</p>	<p>APL1117-28V :  XXXXX - Date Code</p>
<p>APL1117 -33F/G/U :  XXXXX - Date Code</p>	<p>APL1117-33V :  XXXXX - Date Code</p>

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

## Absolute Maximum Ratings

Symbol	Parameter	Rating <sup>(Note)</sup>	Unit
V <sub>I</sub>	Input Voltage APL1117, APL1117-33 APL1117-18, APL1117-25, APL1117-28	15 9	V
T <sub>J</sub>	Operating Junction Temperature Range Control Section Power Transistor	0 to 125 0 to 150	°C
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead Temperature (Soldering, 10 second)	260	°C

Note : The values here show the absolute maximum rating, and for normal usage please refer the test condition in Electrical Characteristics Table.

## Electrical Characteristics

Unless otherwise noted, these specifications apply over  $C_{IN} = 10\mu F$ ,  $C_{OUT} = 10\mu F$ , and  $T_A = 0$  to  $70^\circ C$ . Typical values refer to  $T_A = 25^\circ C$ .

Symbol	Parameter	Test Conditions	APL1117			Unit
			Min.	Typ.	Max.	
$V_{REF}$	Reference Voltage	$10mA \leq I_{OUT} \leq 1A$ , $1.4V \leq (V_{IN} - V_{OUT}) \leq 10.75V$ , $T_J = 0 \sim 125^\circ C$	1.225	1.250	1.275	V
$V_{OUT}$	Output Voltage					
	APL1117-18	$T_J = 0 \sim 125^\circ C$ , $0 \leq I_{OUT} \leq 1.5A$ , $3.25V \leq V_{IN} \leq 9V$ ,	1.764	1.800	1.836	V
	APL1117-25	$T_J = 0 \sim 125^\circ C$ , $0 \leq I_{OUT} \leq 1A$ , $3.95V \leq V_{IN} \leq 9V$ ,	2.450	2.500	2.550	
	APL1117-28	$T_J = 0 \sim 125^\circ C$ , $0 \leq I_{OUT} \leq 1A$ , $4.25V \leq V_{IN} \leq 9V$ ,	2.790	2.850	2.910	
	APL1117-33	$T_J = 0 \sim 125^\circ C$ , $0 \leq I_{OUT} \leq 1A$ , $4.75V \leq V_{IN} \leq 12V$ ,	3.235	3.300	3.365	
$REG_{LINE}$	Line Regulation					
	APL1117	$I_{OUT} = 10mA$ , $1.5V \leq (V_{IN} - V_{OUT}) \leq 10.75V$ (Note1)		0.03	0.2	% mV
	APL1117-18	$I_{OUT} = 0A$ , $3.25V \leq V_{IN} \leq 9V$ (Note1)		1	6	
	APL1117-25	$I_{OUT} = 0A$ , $3.95V \leq V_{IN} \leq 9V$ (Note1)		1	6	
	APL1117-28	$I_{OUT} = 0A$ , $4.25V \leq V_{IN} \leq 9V$ (Note1)		1	6	
	APL1117-33	$I_{OUT} = 0A$ , $4.75V \leq V_{IN} \leq 12V$ (Note1)		1	6	
$REG_{LOAD}$	Load Regulation					
	APL1117	$(V_{IN} - V_{OUT}) = 3V$ , $0 \leq I_{OUT} \leq 1A$ (Note1)		0.1	0.4	% mV
	APL1117-18	$V_{IN} = 3.25V$ , $0 \leq I_{OUT} \leq 1A$ (Note1)		1	10	
	APL1117-25	$V_{IN} = 3.95V$ , $0 \leq I_{OUT} \leq 1A$ (Note1)		1	10	
	APL1117-28	$V_{IN} = 4.25V$ , $0 \leq I_{OUT} \leq 1A$ (Note1)		1	10	
	APL1117-33	$V_{IN} = 4.75V$ , $0 \leq I_{OUT} \leq 1A$ (Note1)		1	10	
$V_D$	Dropout Voltage	$I_{OUT} = 100mA$ (Note2) $I_{OUT} = 500mA$ (Note2) $I_{OUT} = 1A$ (Note2)		1 1.05 1.1	1.1 1.2 1.3	V
$I_{LIMIT}$	Current Limit	$(V_{IN} - V_{OUT}) = 5V$ , $T_J = 25^\circ C$	1000			mA
$I_{ADJ}$	Adjust Pin Current APL1117	$(V_{IN} - V_{OUT}) = 3V$ , $I_{OUT} = 10mA$		60	120	$\mu A$
$\Delta I_{ADJ}$	Adjust Pin Current Change APL1117	$10mA \leq I_{OUT} \leq 1A$ , $1.4V \leq (V_{IN} - V_{OUT}) \leq 10.75V$		0.2	5	$\mu A$
$I_O$	Minimum Load Current APL1117	$(V_{IN} - V_{OUT}) = 10.75V$ (Note3)		1.7		mA
PSRR	Ripple Rejection	$f_{RIPPLE} = 120Hz$ , $V_{RIPPLE} = 1V_{P-P}$ , $(V_{IN} - V_{OUT}) = 3V$	60	75		dB
$T_R$	Thermal Regulation	$T_J = 25^\circ C$ , 30ms Pulse		0.01	0.02	%/W
$T_S$	Temperature Stability			0.5		%
$L_S$	Long -Term Stability	$T_J = 125^\circ C$ , 1000Hrs.		0.3		%
$V_N$	RMS Output Noise	$T_J = 25^\circ C$ , $10Hz \leq F \leq 10kHz$ , (% of $V_{OUT}$ )		0.003		%

## Electrical Characteristics (Cont.)

Unless otherwise noted , these specifications apply over  $C_{IN}= 10\mu F$  ,  $C_{OUT}= 10\mu F$  , and  $T_A= 0$  to  $70^{\circ}C$ . Typical values refer to  $T_A= 25^{\circ}C$ .

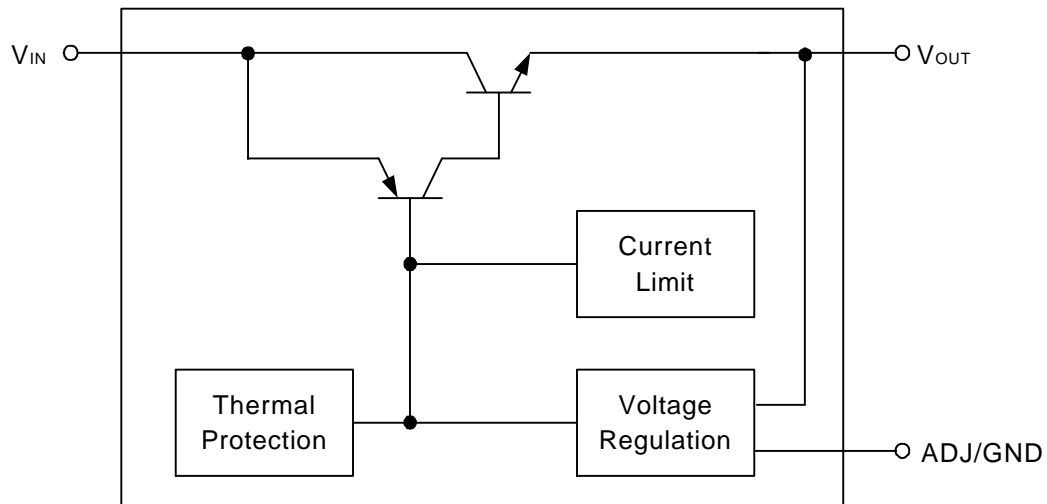
Symbol	Parameter	Test Conditions	APL1117			Unit
			Min.	Typ.	Max.	
$\theta_{th}$	Thermal Resistance	Junction to Case, at Tab Junction to Ambient		15 50		$^{\circ}C/ W$
OT	Over Temperature Point			150		$^{\circ}C$
$I_q$	Quiescent Current					
	APL1117-18	$V_{IN}\leq 9V$		5.5	10	mA
	APL1117-25	$V_{IN}\leq 9V$		5.5	10	
	APL1117-28	$V_{IN}\leq 9V$		5.5	10	
	APL1117-33	$V_{IN}\leq 12V$		5.5	10	

Note 1 : See thermal regulation specifications for changes in output voltage due to heating effects. Load line regulations are measured at a constant junction temperature by low duty cycle pulse testing.

Note 2 : Dropout voltage is specified over the full output current range of the device. Dropout voltage is defined as the minimum input/output differential measured at the specified output current. Test points and limits are also shown on the Dropout Voltage curve.

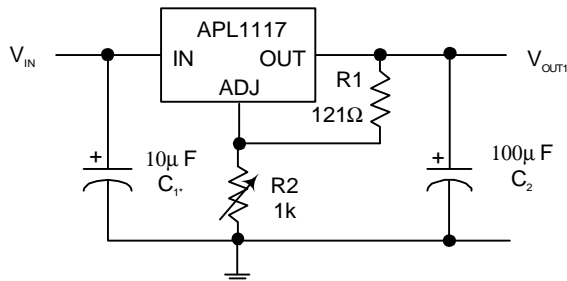
Note 3 : Minimum load current is defined as the minimum output current required to maintain regulation.

## Block Diagram



## Application Circuits

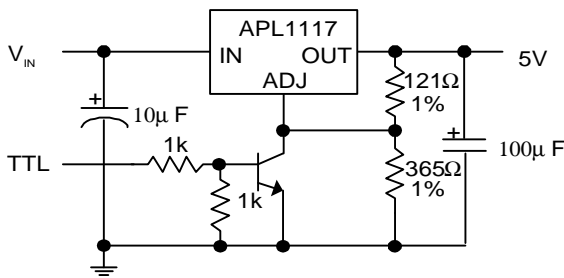
### 1.25V to 10.7V Adjustable Regulator



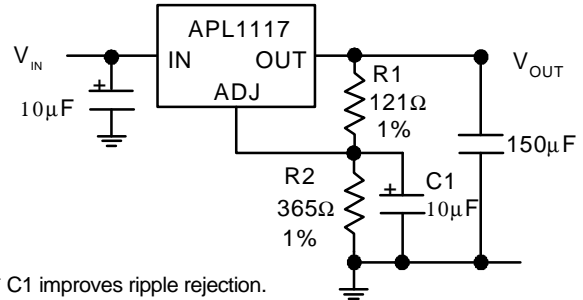
\* Needed if device is far from filter capacitors

$$V_{OUT} = 1.250V \times \frac{R1 + R2}{R1}$$

### 5V Regulator with Shutdown



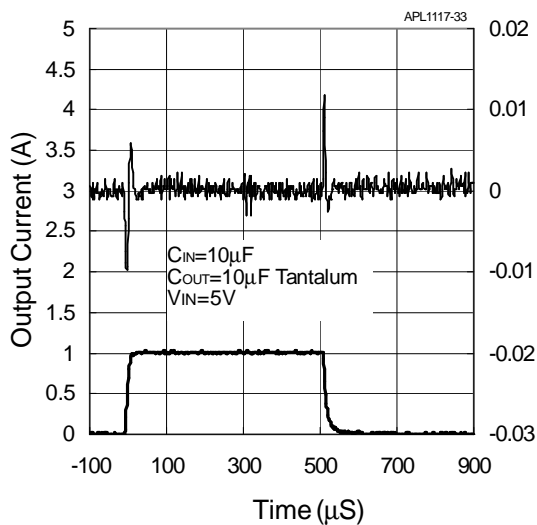
### Improving Ripple Rejection



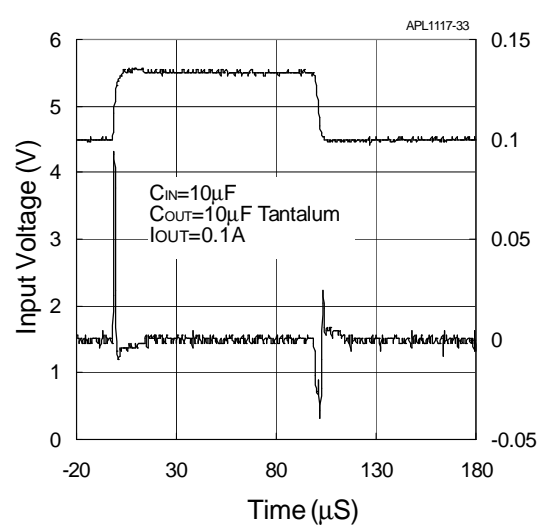
\* C1 improves ripple rejection.  
X<sub>C</sub> should be approximately equal to R1 at ripple frequency

## Typical Characteristics

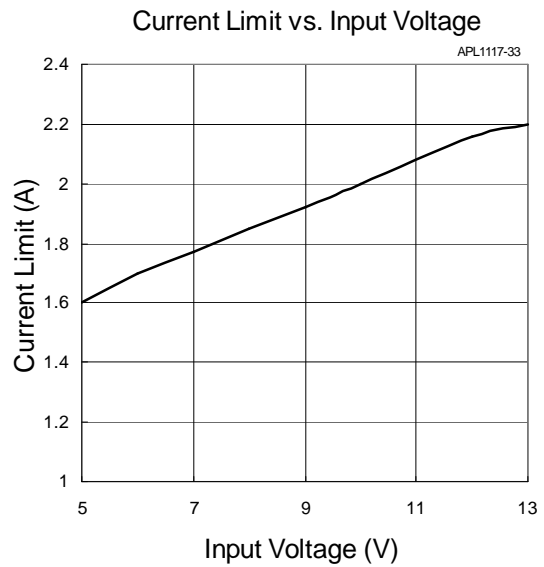
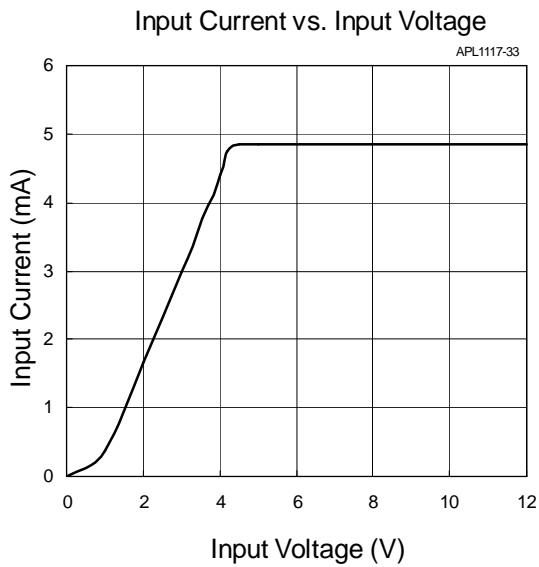
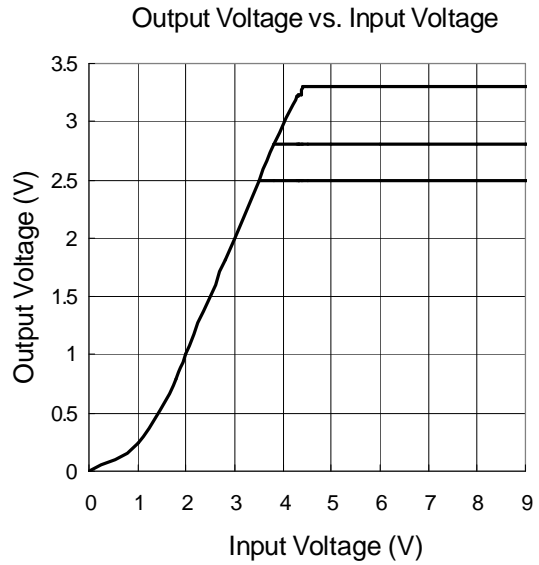
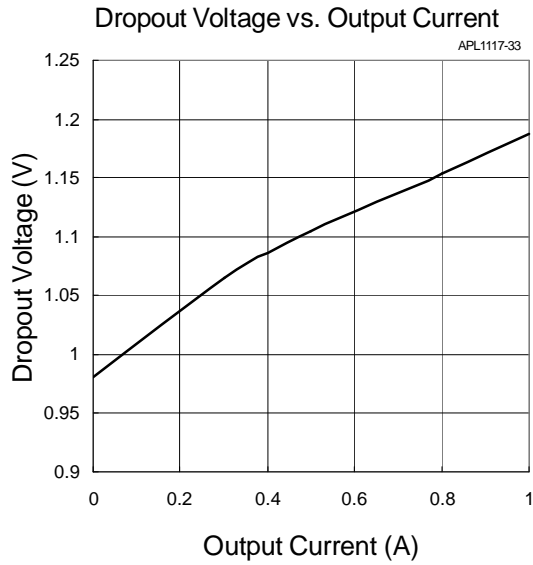
### Load Transient Response



### Line Transient Response

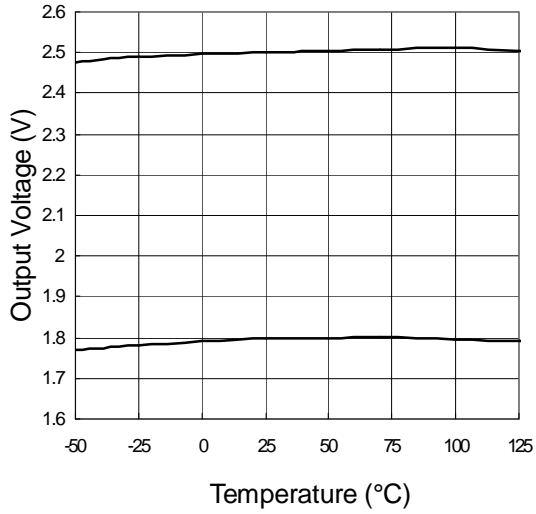


## Typical Characteristics

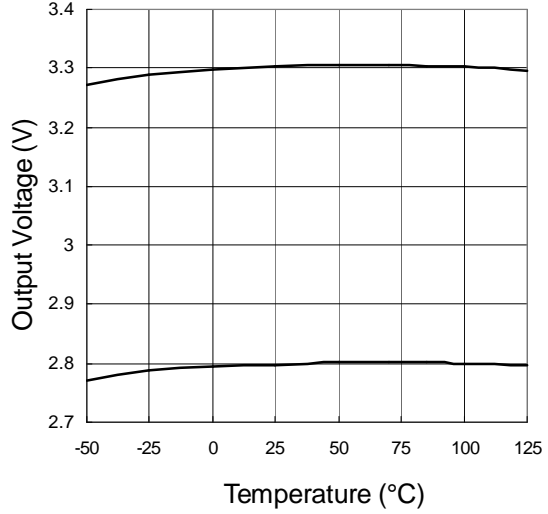


Typical Characteristics (Cont.)

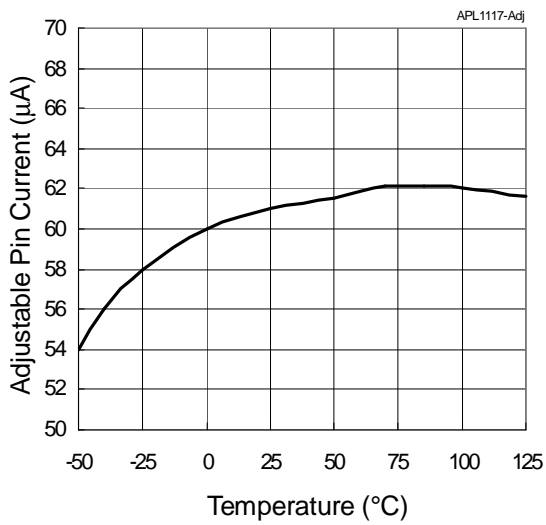
Output Voltage vs. Temperature



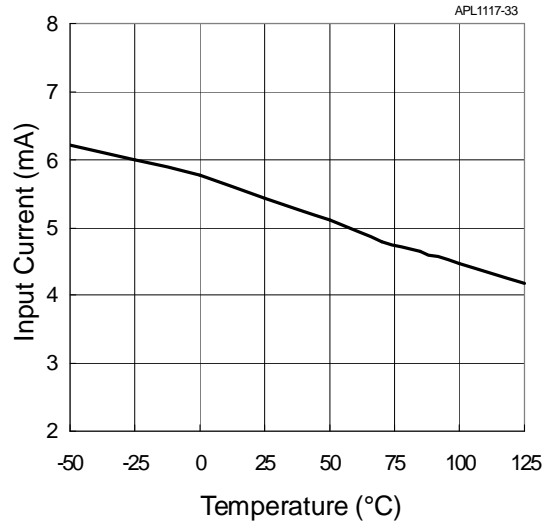
Output Voltage vs. Temperature



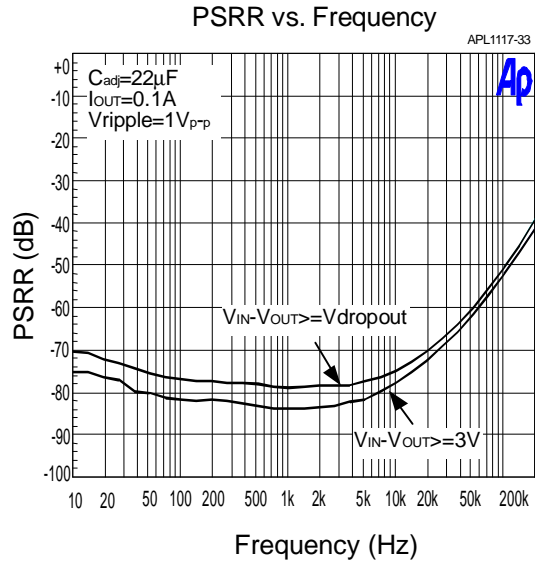
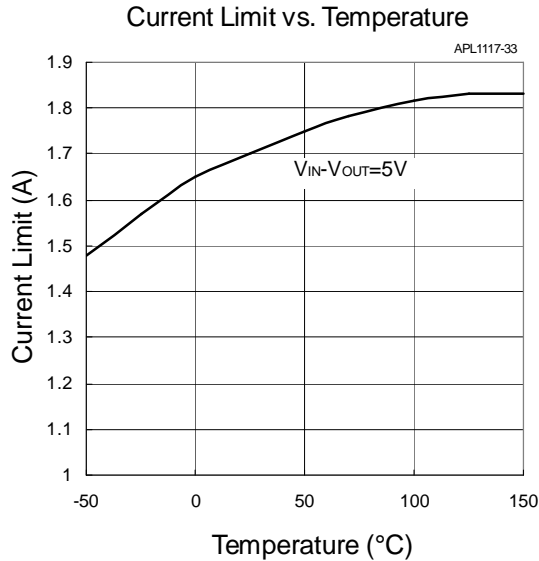
Adjustable Pin Current vs. Temperature



Input Current vs. Temperature



## Typical Characteristics Cont.



## Application Information

### Output Voltage

The APL1117 develops a 1.25V reference voltage between the output and the adjust terminal. By placing a resistor between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is chosen to be the specified minimum load current of 10mA. For fixed voltage devices R1 and R2 are included in the device.

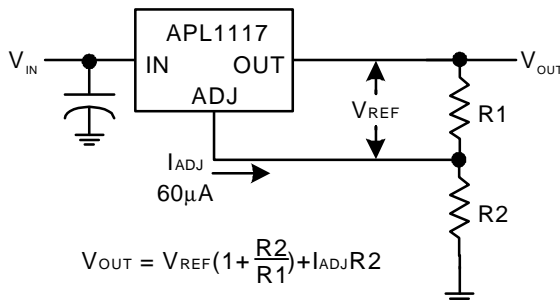


Figure 1. Basic Adjustable Regulator

### Load Regulation

When the adjustable regulator is used, load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the output pin of the device. Best load regulation is obtained when the top of the resistor divider (R1) is tied directly to the output pin of the device, not to the load. For fixed voltage devices the top of R1 is internally connected to the output, and the ground pin can be connected to low side of the load. If R1 were connected to the load,  $R_p$  is multiplied by the divider ratio, the effective resistance between the regulator and the load would be:

$$R_p \times \left(1 + \frac{R_2}{R_1}\right), R_p = \text{Parasitic Line Resistance}$$



## Application Information (Cont.)

### Load Regulation (Cont.)

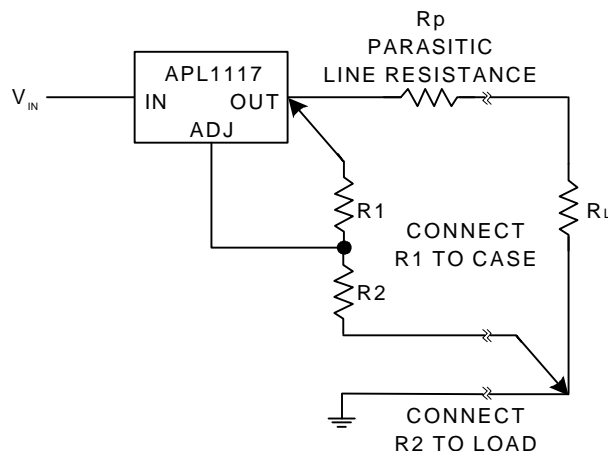


Figure 2. Connections for Best Load Regulation

### Input Capacitor

An input capacitor of 10 $\mu$ F or greater is recommended. Tantalum, or aluminum electrolytic capacitors can be used for bypassing. Larger Values will improve ripple rejection by bypassing the input to the regulator.

### Output Capacitor

The APL1117 requires an output capacitor to maintain stability and improve transient response. Proper capacitor selection is important to ensure proper operation. The APL1117 output capacitor selection is dependent upon the ESR (equivalent series resistance) of the output capacitor to maintain stability. When the output capacitor is 10 $\mu$ F or greater, the output capacitor should have an ESR less than 1 $\Omega$ . This will improve transient response as well as promote stability. A low-ESR solid tantalum capacitor works extremely well and provides good transient response and stability over temperature.

Aluminum electrolytics can also be used, as long as the ESR of the capacitor is <1 $\Omega$ . The value of the output capacitor can be increased without limit. Higher capacitance values help to improve transient response and ripple rejection and reduce output noise.

### Ripple Rejection

The curves for Ripple Rejection were generated using an adjustable device with the adjust pin bypassed. With a 22 $\mu$ F bypassing capacitor 75dB ripple rejection is obtainable at any output level. The impedance of the adjust pin capacitor, at the ripple frequency, should be < R1. R1 is normally in the range of 100 $\Omega$ -200 $\Omega$ . The size of the required adjust pin capacitor is a function of the input ripple frequency. At 120Hz, with R1=100 $\Omega$ , the adjust pin capacitor should be 13 $\mu$ F. For fixed voltage devices, and adjustable devices without an adjust pin capacitor, the output ripple will increase as the ratio of the output voltage to the reference voltage ( $V_{OUT}/V_{REF}$ ).

### Thermal Considerations

The APL1117 regulators have thermal protection to limit junction temperature to 150 $^{\circ}$ C. However, device functionality is only guaranteed to a maximum junction temperature of +125 $^{\circ}$ C.

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Figure 3&4 show for the TO-252 and SOT-223 the measured values  $\theta_{(J-A)}$  for different copper area sizes using a 2 layers, 1.6mm, and 6Sq. cm FR-4 PCB with 2oz. copper and a ground plane layer on the backside area used for heatsinking. It can be used as a rough guideline in estimating thermal resistance. Both the TO-252 and SOT-223 packages use a copper plane on the PCB and the PCB itself as a heatsink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the package to the plane.

## Application Information (Cont.)

### Thermal Considerations (Cont.)

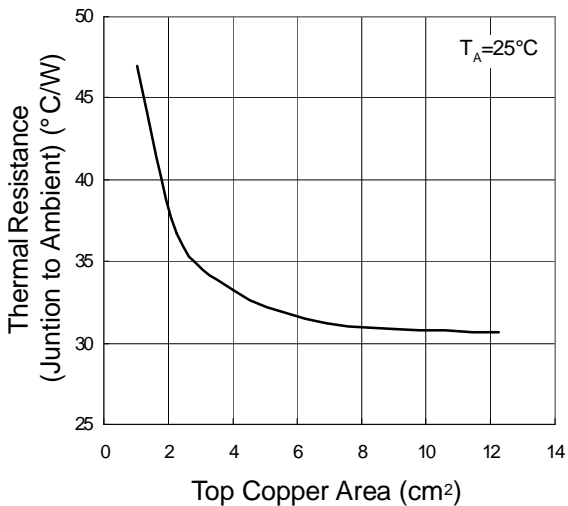


Figure 3.

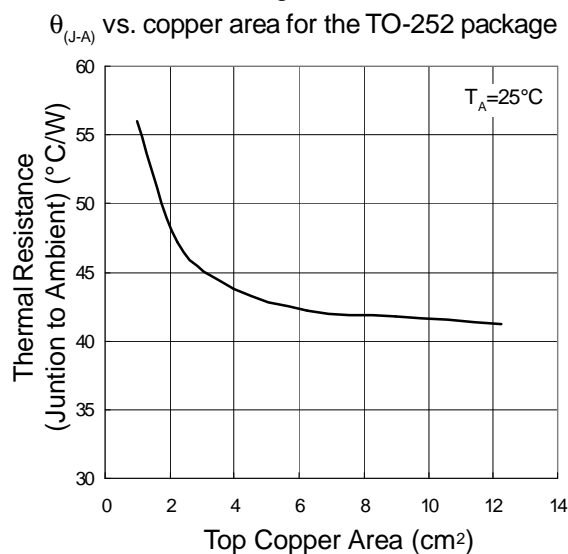


Figure 4.

$\theta_{(J-A)}$  vs. copper area for the SOT-223 package

The thermal resistance for each application will be affected by thermal interactions with other components on the board. Some experimentation will be necessary to determine the actual value.

The power dissipation of APL1117 is equal to :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Maximum junction temperature is equal to :

$$T_{JUNCTION} = T_{AMBIENT} + (P_D \times \theta_{JA})$$

Note:  $T_{JUNCTION}$  must not exceed 125°C

### Safe Operation Area

Using the experiment result of previous Thermal Consideration (choose the one with 1.5cm \* 1.5cm polygen area) and  $\theta_{(J-A)} = 50^\circ\text{C/W}$  spec, the safe operation area of APL1117 in TO-252 and SOT-223 packages can be obtained as Figure 5.

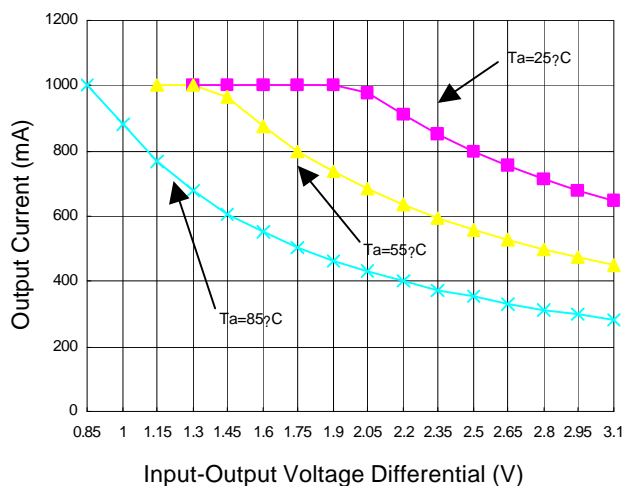
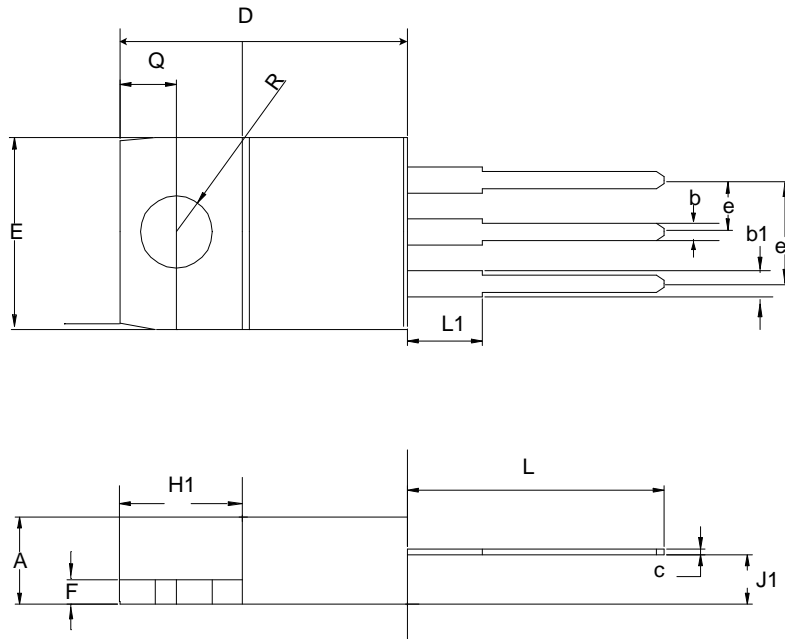


Figure 5.

Safe Operation Area of APL1117 in TO-252 and SOT-223 packages (limited by Power Dissipation with  $T_{JUNCTION} < 125^\circ\text{C}$ )

## Package Information

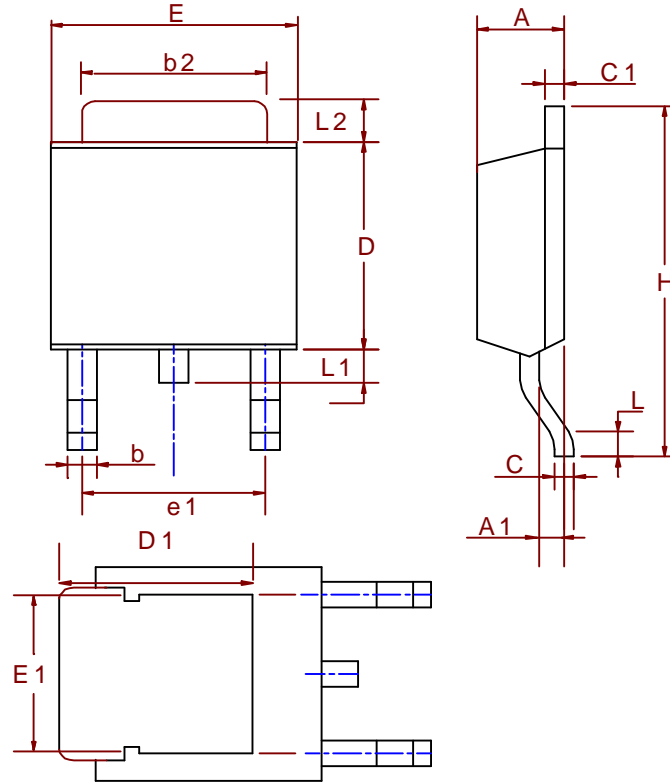
TO-220 ( Reference JEDEC Registration TO-220)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	3.56	4.83	0.140	0.190
b1	1.14	1.78	0.045	0.070
b	0.51	1.14	0.020	0.045
c	0.31	1.14	0.012	0.045
D	14.23	16.51	0.560	0.650
e	2.29	2.79	0.090	0.110
e1	4.83	5.33	0.190	0.210
E	9.65	10.67	0.380	0.420
F	0.51	1.40	0.020	0.055
H1	5.84	6.86	0.230	0.270
J1	2.03	2.92	0.080	0.115
L	12.7	14.73	0.500	0.580
L1	3.65	6.35	0.143	0.250
R	3.53	4.09	0.139	0.161
Q	2.54	3.43	0.100	0.135

## Package Informaion

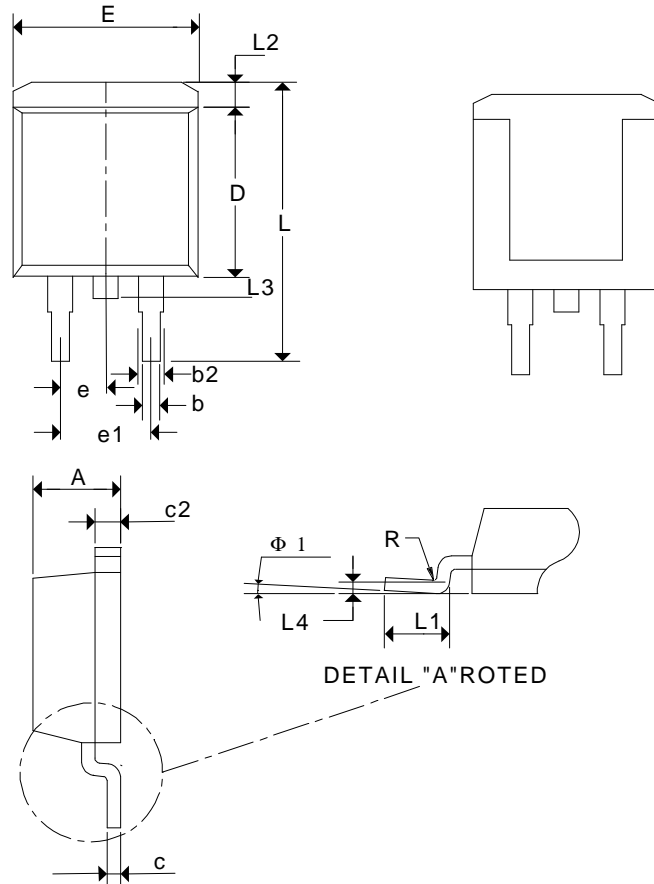
TO-252 (Reference JEDEC Registration TO-252)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.18	2.39	0.086	0.094
A1	0.89	1.27	0.035	0.050
b	0.508	0.89	0.020	0.035
b2	5.207	5.461	0.205	0.215
C	0.46	0.58	0.018	0.023
C1	0.46	0.58	0.018	0.023
D	5.334	6.22	0.210	0.245
D1	5.2 REF		0.205 REF	
E	6.35	6.73	0.250	0.265
E1	5.3 REF		0.209 REF	
e1	3.96	5.18	0.156	0.204
H	9.398	10.41	0.370	0.410
L	0.51		0.020	
L1	0.64	1.02	0.025	0.040
L2	0.89	2.032	0.035	0.080

## Package Information

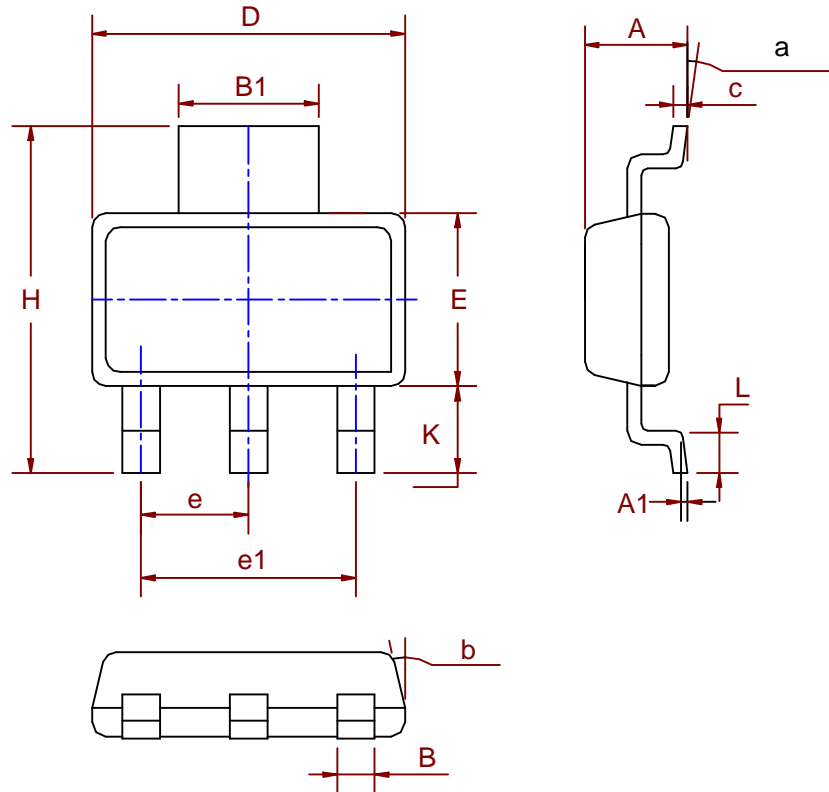
TO-263 (Reference JEDEC Registration TO-263)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.06	4.83	0.160	0.190
b	0.51	1.016	0.02	0.040
b2	1.14	1.651	0.045	0.065
c	0.38 TYP.		0.015 TYP.	
c2	1.14	1.40	0.045	0.055
D	8.64	9.65	0.340	0.380
e	2.54 TYP		0.100 TYP	
e1	4.83	5.33	0.190	0.210
L	14.60	15.88	0.575	0.625
L1	2.24	2.84	0.090	0.110
L2	1.02	2.92	0.040	0.112
L3	1.20	1.78	0.050	0.070

## Package Information

SOT-223 (Reference JEDEC Registration SOT-223)

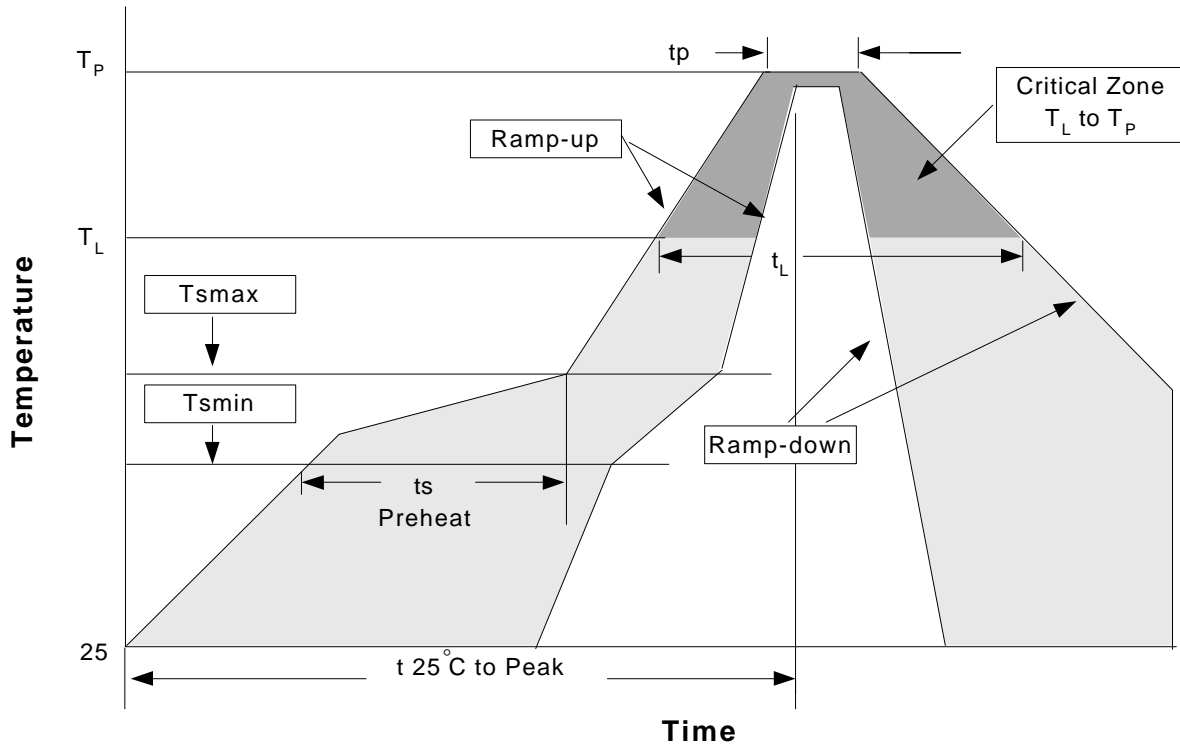


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.50	1.80	0.059	0.070
A1	0.02	0.08	0.001	0.003
B	0.60	0.80	0.023	0.031
B1	2.90	3.10	0.113	0.121
c	0.28	0.32	0.011	0.012
D	6.30	6.70	0.246	0.261
E	3.30	3.70	0.129	0.144
e	2.3 BSC		0.090 BSC	
E1	4.6 BSC		0.179 BSC	
H	6.70	7.30	0.261	0.285
L	0.91	1.10	0.035	0.043
K	1.50	2.00	0.059	0.078
α	0°	10°	0°	10°
β	13°		°13	

## Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb)
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.
Packaging	2500 devices per reel

### Reflow Condition (IR/Convection or VPR Reflow)



### Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate ( $T_L$ to $T_P$ )	3°C/second max.	3°C/second max.
Preheat		
- Temperature Min ( $T_{smin}$ )	100°C	150°C
- Temperature Max ( $T_{smax}$ )	150°C	200°C
- Time (min to max) ( $t_s$ )	60-120 seconds	60-180 seconds
Time maintained above:		
- Temperature ( $T_L$ )	183°C	217°C
- Time ( $t_L$ )	60-150 seconds	60-150 seconds
Peak/Classification Temperature ( $T_P$ )	See table 1	See table 2
Time within 5°C of actual Peak Temperature ( $t_p$ )	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

## Classification Reflow Profiles(Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

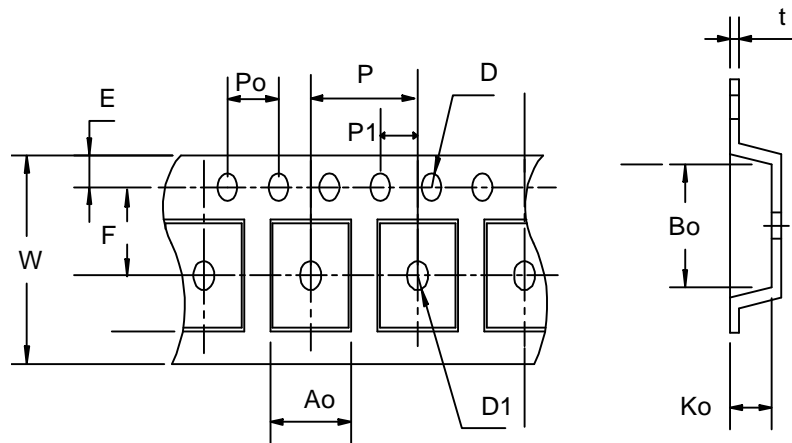
Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

\*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

## Reliability test program

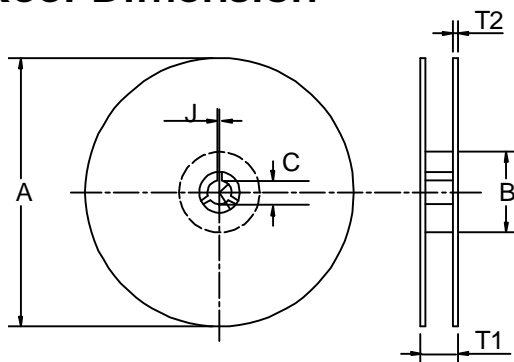
Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I <sub>tr</sub> > 100mA

## Carrier Tape & Reel Dimension





## Carrier Tape & Reel Dimension



Application	A	B	C	J	T1	T2	W	P	E
TO-252	330 ± 3	100 ± 2	13 ± 0.5	2 ± 0.5	16.4 +0.3 -0.2	2.5 ± 0.5	16 +0.3 -0.1	8 ± 0.1	1.75 ± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	7.5 ± 0.1	1.5 +0.1	1.5 ± 0.25	4.0 ± 0.1	2.0 ± 0.1	6.8 ± 0.1	10.4 ± 0.1	2.5 ± 0.1	0.3 ± 0.05
Application	A	B	C	J	T1	T2	W	P	E
TO-263	380 ± 3	80 ± 2	13 ± 0.5	2 ± 0.5	24 ± 4	2 ± 0.3	24 +0.3 -0.1	16 ± 0.1	1.75 ± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	11.5 ± 0.1	1.5 +0.1	1.5 ± 0.25	4.0 ± 0.1	2.0 ± 0.1	10.8 ± 0.1	16.1 ± 0.1	5.2 ± 0.1	0.35 ± 0.013
Application	A	B	C	J	T1	T2	W	P	E
SOT-223	330 ± 1	62 ± 1.5	12.75 ± 0.15	2 ± 0.6	12.4 +0.2	2 ± 0.2	12 ± 0.3	8 ± 0.1	1.75 ± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5 ± 0.05	1.5 +0.1	1.5 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	6.9 ± 0.1	7.5 ± 0.1	2.1 ± 0.1	0.3 ± 0.05

(mm)

## Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
TO- 252	16	13.3	2500
TO- 263	24	21.3	1000
SOT- 223	12	9.3	2500

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