Features

- **10-bit Resolution**
- **2 Gsps Sampling Rate**
- **Fully Compatible with AT84AS003 10-bit 1.5 Gsps ADC with DMUX**
- **Selectable 1:2 or 1:4 Demultiplexed Output**
- **500 mVpp Differential 100Ω or Single-ended 50Ω Analog Input**
- **100Ω Differential or Single-ended 50Ω Clock input**
- **LVDS Output Compatibility**
- **Functions:**
  - **ADC Gain Adjust**
  - **Sampling Delay Adjust**
  - **1:4 Demultiplexed Simultaneous or Staggered Digital Outputs**
  - **Data Ready Output with Asynchronous Reset**
  - **Out-of-range Output Bit (11th Bit)**
- **Power Consumption : 6.5W**
- **Power Supplies: -5V, -2.2V, 3.3V and V_{PLUSD} Output Power Supply**
- **Package**
  - **Cavity Down EBGA 317 (Enhanced Ball Grid Array)**
  - **25 × 35 mm Overall Dimensions**

Performances

- 3.3 GHz Full-power Analog Input Bandwidth
- ±0.2 dB Gain Flatness from DC up to 1.5 GHz
- Single-tone Performance at Fs = 2 Gsps, Full First Nyquist Zone
  - ENOB = 7.8 Effective Bits, F_{IN} = 1000 MHz
  - SNR = 51 dB, SFDR = -55 dBFS, F_{IN} = 1000 MHz
- Dual-tone Performance (IMD3) at Fs = 1.7 Gsps (-7 dBFS each tone)
  - Fin1 = 995 MHz, Fin2 = 1005 MHz: IMD3 = -60 dBFS
  - Fin1 = 1545 MHz, Fin2 = 1555 MHz: IMD3 = -60 dBFS

Screening

- Temperature Range:
  - T_C > 0°C; T_J < 90°C (Commercial “C” Grade)
  - T_C > -20°C; T_J < 110°C (Industrial “V” Grade)

Applications

- Direct RF Down Conversion
- Ultra Wide Band Satellite Receivers
- Radars and Countermeasures
- High-speed Acquisition Systems
- High Energy Physics
- Automatic Test Equipment

10-bit 2 Gsps ADC With 1:4 DMUX

AT84AS004

Summary

5431AS–BDC–07/05

Note: This is a summary document. A complete document is not available at this time. For more information, please contact your local Atmel sales office.

1. Description

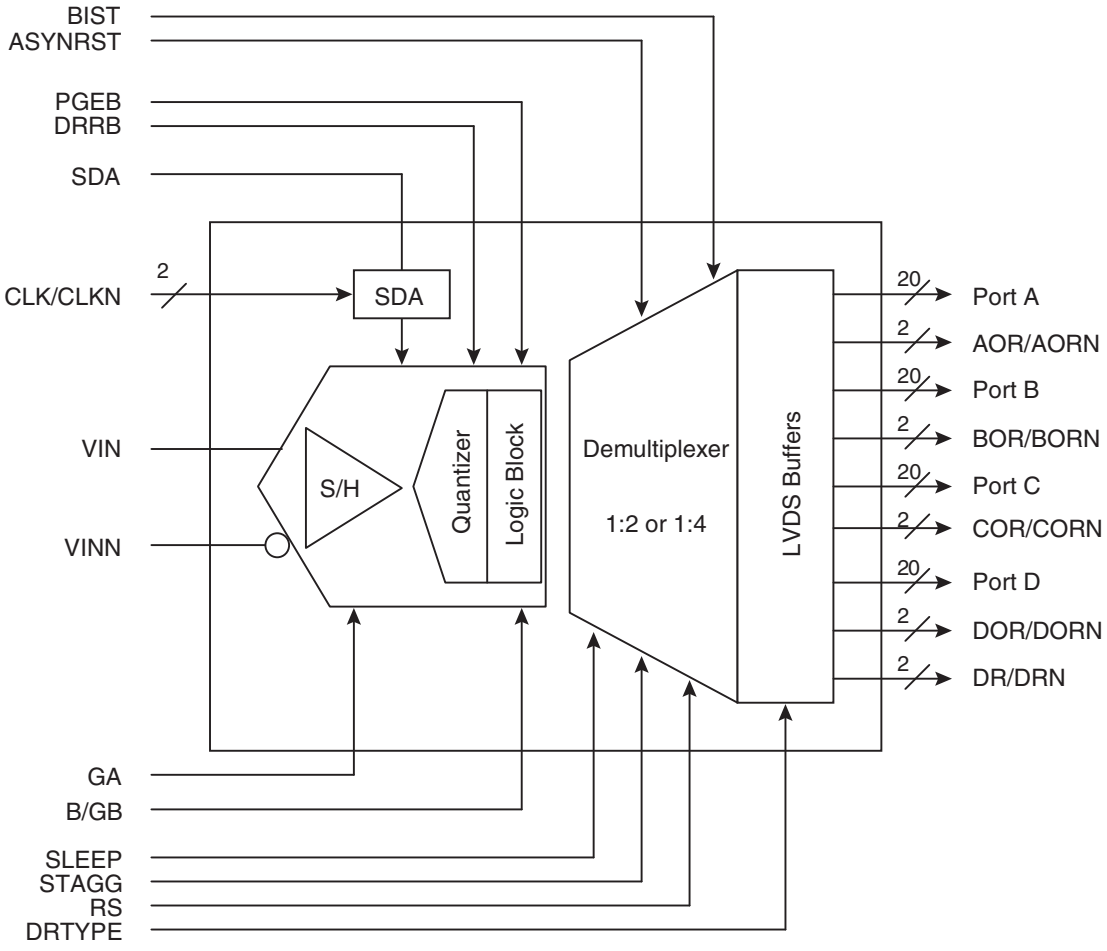
The AT84AS004 combines a 10-bit 2 Gsps analog-to-digital converter with a 1:4 DMUX, designed for accurate digitization of broadband signals.

It features 7.8 Effective Number of Bits (ENOB) and -55 dBFS Spurious Free Dynamic Range (SFDR) at 1.5 Gsps over the full first Nyquist zone.

The 1:4 demultiplexed digital outputs are LVDS logic compatible, allowing easy interfacing with standard FPGAs or DSPs .The AT84AS004 operates at up to 1.5 Gsps, without additional tuning of the synchronization between the ADC and DMUX.

The AT84AS004 comes in a 25 × 35 mm EBGA317 package. This package has the same TCE as FR4 boards, offering excellent reliability when subjected to large thermal variations.

Figure 1. Block Diagram



2. Functional Description

The AT84AS004 is a 10-bit 2 Gsps ADC combined with a high-speed demultiplexer (DMUX) used to lower the LVDS output bit stream (10-bit data and one out-of range bit) by a factor of 2 or 4. It is fully compatible with the AT84AS003 10-bit 1.5 Gsps ADC.

The ADC works in fully differential mode from the analog input to the digital outputs. It provides an on-chip 100Ω differential termination for the clock input. The analog input is 500 mVpp on a 100Ω differential input impedance. 50Ω reverse terminations are required for the analog input. They should be placed as close as possible to the EBGA package input pins (2 mm maximum). The output clock and the output data are LVDS compatible (100Ω differentially terminated).

The AT84AS004 ADC features two asynchronous resets:

- DRRB, which ensures that the first digitized data corresponds to the first acquisition
- ASYNCRST, which initializes the DMUX

The gain control pin GA is used to finely adjust the ADC gain to a unity gain.

The control pin B/GB is provided to select either a binary or gray data output format.

A Sampling Delay Adjust function (SDA, activated via the SDAEN signal) may be used to fine-tune the ADC aperture delay by approximately 120 ps around its nominal value. This function is useful when interleaving multiple ADCs.

The control pin B/GB is provided to select either a binary or Gray data output format.

A tunable delay cell (controlled via CLKDACTRL) is integrated between the ADC and the DMUX on the clock path to fine-tune the data according to the clock alignment at the interface between the ADC and the DMUX. This delay can be tuned from -250 to 250 ps around a default center value, featuring a 500 ps typical tuning range. No tuning should be necessary for operating frequencies up to 1.5 Gsps.

An extra stand-alone delay cell is also provided. It is controlled via analog DACTRL control input and activated via DAEN. The tuning range is typically 500 ps.

A pattern generator (PGEB) is integrated in the ADC block for debugging purposes or acquisition setup. Similarly, a Built-in Self Test (BIST) is provided for quick debug of the DMUX block.

The demultiplexer ratio can be selected using RS (1:2 or 1:4 ratio).

Two modes for the output clock (via DRTYPE) are selectable:

- DR mode: only the output clock's rising egde is active, the output clock rate is the same as the output data rate
- DR/2 mode: both the output clock's rising and falling edges are active, the output clock rate is half the output data rate

The AT84AS004's data is output in two different modes:

- Staggered: even and odd bits are output with half a data period delay
- Simultaneous: even and odd bits are output at the same time

A sleep mode is provided to lower the power consumption of the DMUX block.

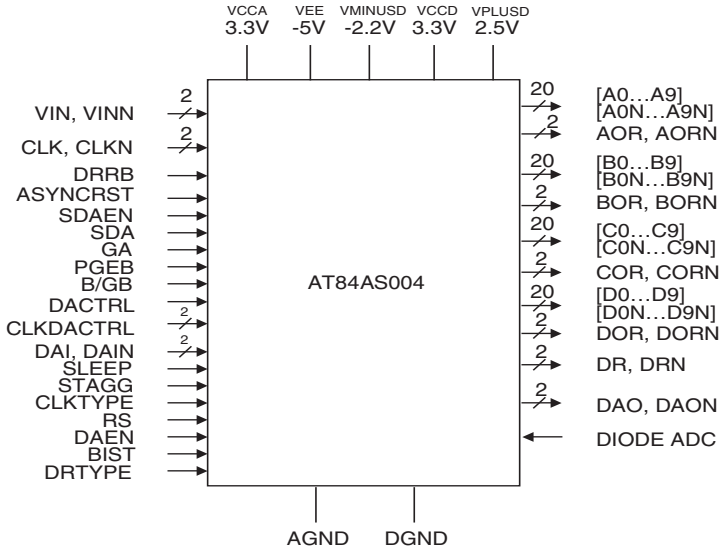
Die junction temperature monitoring is also provided to facilitate management of the junction temperature, by sensing the voltage drop across one diode implemented on the ADC , close to the chip's hot point.

The AT84AS004 is delivered in an Enhanced Ball Grid Array (EBGA). Its TCE, which is similar to that of the FR4 material, makes it highly suitable for applications exposed to large thermal variations.

Table 2-1. Description of Functions

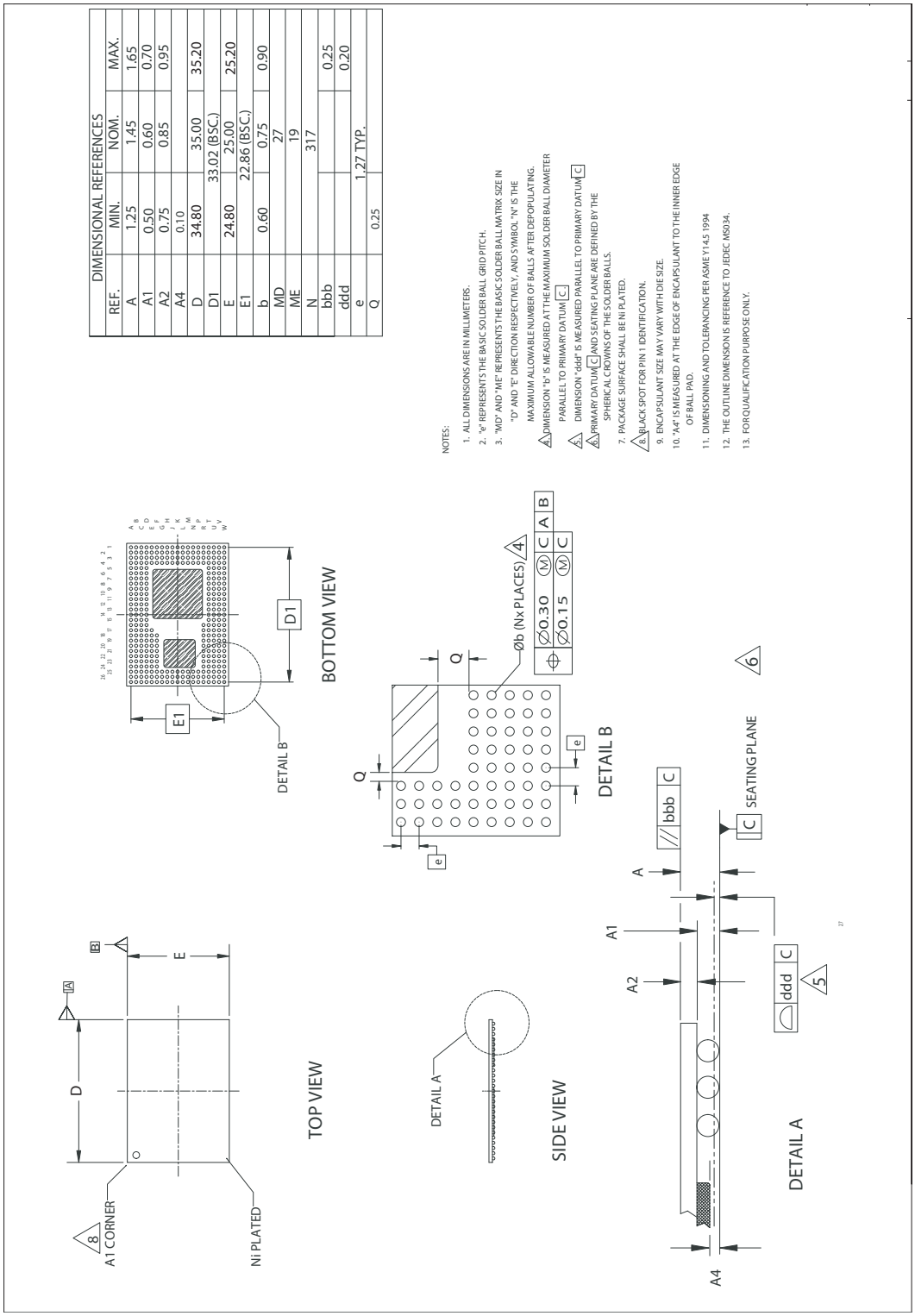
Name	Function	Name	Function
V_{CCA}	Analog 3.3V power supply	DOR/ DORN/ DRD/DRDN	Additional output bit port D or port D output clock in staggered mode
V_{CCD}	Digital 3.3V power supply	RS	DMUX ratio selection signal
V_{EE}	Analog -5V power supply	CLKDACTRL	Control signal for clock delay cell
V_{MINUSD}	Digital -2.2V power supply	DACTRL	Control signal for standalone delay cell
V_{PLUSD}	Output 2.5 power supply	DAEN	Enable signal for standalone delay cell
AGND	Analog ground	DAI, DAIN	Input signals for standalone delay cell
DGND	Digital ground	DAO, DAON	Output signals for standalone delay cell
CLK, CLKN	Input clock signals	GA	ADC gain adjust
VIN, VINN	Analog input data	SDA	ADC sampling delay adjust
DRRB	ADC reset	SDAEN	ADC SDA enable
ASYNCRST	DMUX asynchronous reset	PGEB	ADC pattern generator
DR/DRN	Output clock signals	B/GB	Binary or gray output code selection
A0…A9 A0N…A9N	Output data port A	SLEEP	Sleep mode selection signal
AOR, AORN	Additional output bit port A or Port A output clock in staggered mode	STAGG	Staggered mode selection for data outputs
B0…B9 B0N…B9N	Output data port B	CLKTYPE	Input clock type selection signal
BOR/ BORN/ DRB/DRBN	Additional output bit port B or port B output clock in staggered mode	DRTYPE	Output clock type selection signal
C0…C9 C0N…C9N	Output data port C	BIST	Built-in self test
COR/CORN/ DRC/DRCN	Additional output bit port C or port C output clock in staggered mode	DIODE ADC	Diode for die junction temperature monitoring (ADC)
D0…D9 D0N…D9N	Output data port D		

Figure 2-1. Device Pinout



3. Package Information

Figure 2. EBGA 317 Package Outline (Bottom View)



4. Ordering Information

Part Number	Package	Temperature Range	Screening	Comments
AT84XAS004TP	EBGA 317	Ambient	Prototype	Prototype version Please contact your local Atmel sales office
AT84AS004CTP	EBGA 317	Commercial “C” T_C > 0°C; T_J < 90°C	Standard	
AT84AS004VTP	EBGA 317	Industrial “V” T_C> -20°C; T_J < 110°C	Standard	
AT84AS004TP-EB	EBGA 317	Ambient	Prototype	Evaluation kit

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